REMARKS

Non-elected claims 1-15 are cancelled above.

Claims 16 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa, *et al.* (U.S. Publication Number 2003/0012117). Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Kai, *et al.* (U.S. Patent Number 6,746,914). Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshitomi (U.S. Patent Number 6,740,974). Claims 17-20, 23 and 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kai, *et al.* in view of Ogawa, *et al.* Claims 14-26 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshitomi in view of Ning, *et al.* (U.S. Patent Number 6,750,115). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 16-33, a dual damascene interconnection structure with a metal-insulator-metal includes a via level intermetal dielectric and a trench level intermetal dielectric which are sequentially stacked on a substrate. A dual damascene interconnection is formed in the via-level intermetal dielectric and the trench-level intermetal dielectric. The dual damascene interconnection includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric. A metal-insulator-metal capacitor is formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer and an upper electrode. The dual damascene interconnection is substantially electrically isolated from the metal-insulator-metal capacitor. An upper metal interconnection is formed on and connected to the upper electrode.

Claims 16-33 are amended to clarify that the dual damascene interconnection includes the upper metal interconnection formed on and connected to the upper electrode and that the dual damascene interconnection is substantially electrically isolated from the metal-insulator-metal capacitor. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

With regard to the rejection of claims 1 and 27 as being anticipated by Ogawa, *et al.*, Ogawa, *et al.* discloses, at page 1, paragraph [0006], that when contact holes that are in contact with an upper electrode provided on a capacitive insulating film of a metal-insulator-metal (MIM) capacitor are formed, the characteristics of the capacitor may be

adversely affected. In Ogawa, *et al.*, at page 4, paragraph [0043], by connecting the upper electrode 35a to an upper interconnect 42 via conductor sidewall 40, dummy lower electrode 33b, dummy cell plug 30 and local interconnect 21b, no plug is needed in contact with the upper electrode 35a or the upper electrode extension 35b.

Ogawa, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, the dual damascene interconnection being substantially electrically isolated from the metal-insulator-metal capacitor, and an upper metal interconnection which is formed on and connected to an upper electrode of a metal-insulator-metal capacitor, as claimed in claims 16-33. Instead, Ogawa, *et al.* discloses an upper interconnect 42 which is connected to the upper electrode 35a via the conductor sidewall 40, dummy lower electrode 33b, dummy cell plug 30b, 30c and local interconnect 21b. Therefore, the upper interconnect 42 is not formed on the upper electrode 35a. Further, Ogawa, *et al.* does not disclose the dual damascene interconnection as claimed, as the upper interconnect 42 is an upper interconnect connected to the upper electrode, and 30c is an interconnect plug. In addition, the upper interconnect 42 and the interconnect plug 30c are not electrically isolated from the MIM capacitor, but rather are electrically connected via the conductor sidewall 40, dummy lower electrode 33b, dummy cell plug 30b, 30c and local interconnect 21b.

Ogawa, *et al.* fails to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Ogawa, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, the dual damascene interconnection being substantially electrically isolated from the metal-insulator-metal capacitor, and an upper metal interconnection which is formed on and connected to an upper electrode of a metal-insulator-metal capacitor, as claimed in claims 16-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 16 and 27 under 35 U.S.C. 102(b) as being anticipated by Ogawa, *et al.*, is respectfully requested.

With regard to the rejection of claim 21 as being anticipated by Kai, *et al.*, Kai, *et al.* discloses the formation of dual damascene plugs in 14 and 16 in a first layer of dielectric 12 and dual damascene plugs 28 and 30 is a second layer of dielectric material 26. The trench of the dual damascene plug 30 does not extend through the second layer of dielectric 26 to the first layer of dielectric 12.

Therefore, Kai, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Instead, in Kai, *et al.* the trench of the dual damascene plug 30 does not extend through the second layer of dielectric 26 to the first layer of dielectric 12.

Kai, *et al.* fails to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Kai, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claim 21 under 35 U.S.C. 102(e) as being anticipated by Kai, *et al.*, is respectfully requested.

With regard to the rejection of claim 22 as being anticipated by Yoshitomi, Yoshitomi discloses a metal-insulator-metal capacitor 120 formed on a diffusion-preventing film 115, and a third inter-layer film 121 formed on the diffusion-preventing film 115, thus covering the capacitor 120. No trench is formed in the third inter-layer film 121. Further, in Yoshitomi, a trench is formed in a fifth inter-layer film 123 and partially through the fourth inter-layer film 122.

Yoshitomi fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Instead, in Yoshitomi, no trench is formed in the third inter-layer film 121, and therefore the trench does not extend through the trench-level intermetal dielectric to the via-level intermetal dielectric.

Yoshitomi fails to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Yoshitomi fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claim 22 under 35 U.S.C. 102(e) as being anticipated by Yoshitomi, is respectfully requested.

With regard to the rejection of claims 17-20, 23 and 28-33 as being unpatentable over Kai, *et al.* and Ogawa, *et al.*, it is believed that the combination of references is improper, and, therefore, reconsideration of the rejections is requested.

Ogawa, *et al.* explicitly teaches away from the cited combination of Ogawa, *et al.* and Kai, *et al.* Ogawa, *et al.* teaches not forming an upper interconnect on the upper electrode and the benefits thereof. Ogawa, *et al.* states, at page 1, paragraph [0006]-[0007], the disadvantages of "contact holes that are in contact with Pt-electrodes (upper electrodes) provided on the capacitive insulating film." Ogawa, *et al.* states at page 1, paragraph [0008], that an "object of the present invention is to provide a semiconductor memory device with an MIM capacitor having excellent characteristics and a method for fabricating the same by providing a means for forming an interconnect layer which is not in direct contact with, i.e., is indirectly connected to, an upper electrode made of, for example, Pt on an capacitive insulating film" (further see Ogawa, *et al.*, page 1, paragraph [0011]). With regard to the first embodiments of FIGs. 1(a) and 1(b) of Ogawa, *et al.*, Ogawa, *et al.* states, at page 4, paragraph [0043], that the "embodiment is characterized by providing no plug which is in contact with the upper electrode 35a or the upper-electrode extension 35b (the upper barrier metal 36) but by connecting the upper electrode 35a to an upper interconnect (the Cu interconnect 42) via the conductor sidewall 40, dummy lower electrode 33b, dummy cell plug 30 and local interconnect 21b" (further see Ogawa, *et al.*, page 4, paragraphs [0045] and [0046]). Further, with regard to the first embodiment of FIGs. 1(a) and 1(b) of Ogawa, *et al.*, Ogawa, *et al.* states, at page 5, paragraph [0043], column 2, lines 15-17, that "the process step of forming a contact hole reaching to the Pt film 35 is eliminated" (further see page 5, paragraph [0043], column 1, lines 58-60). With regard to embodiment 2 of Ogawa, *et al.*,

Ogawa, *et al.* states at page 6, paragraph [0065], that, in this embodiment, "it is also unnecessary to form a contact hole reaching to the Pt film 35 (the upper barrier metal 36) that constitutes the upper electrode 35a." Further, with regard to Embodiment 3 of Ogawa, *et al.*, Ogawa, *et al.* states, at page 6, paragraph [0070], that "the upper electrode 35a is electrically connected to the Cu interconnect 42 via the dummy lower electrode 33b, dummy lower barrier metal 32b, dummy cell plug 30b, lower dummy cell plug 20c, local interconnect 24, lower interconnect plug 20d and interconnect plug 30c. In this embodiment, it is also unnecessary to form a contact hole reaching to the Pt film 35 (upper barrier metal 36) that constitutes the upper electrode 35a." With regard to Embodiment 4 of Ogawa, *et al.*, Ogawa, *et al.* states at page 6, paragraph [0074], that "it is also unnecessary to form a contact hole reaching to the Pt film 35 (upper barrier metal 36) that constitutes the upper electrode 35a." With regard to Embodiment 5 of Ogawa, *et al.*, Ogawa, *et al.* states, at page 7, paragraph [0081], that "it is also unnecessary to form a contact hole reaching to the Pt film 35 (upper barrier metal 36) that constitutes the upper electrode 35a." With regard to embodiment 6, Ogawa, *et al.* states, at page 9, paragraph [0100], that "it is also unnecessary to form a contact hole reaching to the Pt film 35 (upper barrier metal 36) that constitutes the upper electrode 35a," and, at page 9, paragraph [0110], that, according to this embodiment, "it is possible to eliminate the process step of forming a contact hole reaching to the Pt film 35 (the upper barrier metal 36) that constitutes the upper electrode 35a." Further, Ogawa, *et al.* states, at page 10, paragraph [0121], that the "present invention ensures that the upper electrode is electrically connected to an upper interconnect without exposing the upper electrode."

Hence, Ogawa, *et al.* not only fails to teach or suggest an upper metal interconnection formed on and connected to an upper electrode as claimed, but the reference actually explicitly teaches that such a structure should be avoided. The Ogawa, *et al.* reference teaches an elaborate, complex interconnection structure to connect the interconnect 42 to the upper electrode 35a, to avoid a structure in which an interconnect (such as the dual damascene plug 28 of Kai, *et al.*) is formed on the upper electrode. Therefore, Ogawa, *et al.* explicitly teaches away from the cited combination of Ogawa, *et al.* and Kai, *et al.* Furthermore, because of such explicit teaching away, one of skill in the art would in no way be motivated to make the cited combination. Therefore, it is

respectfully believed that the cited combination of the Kai, *et al.* and Ogawa, *et al.* references is improper.

Furthermore, even if the cited references were combined, the claimed invention does not result. Instead, the result would be two connections to an upper electrode, not a dual damascene interconnection and an upper metal interconnection, as claimed in claims 16-33.

Therefore, Ogawa, *et al.* and Kai, *et al.*, as discussed above, fail to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Ogawa, *et al.* and Kai, *et al.* fail to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, the dual damascene interconnection being substantially isolated from the metal-insulator-metal capacitor, and an upper metal interconnection which is formed on and connected to an upper electrode of a metal-insulator-metal capacitor, as claimed in claims 16-33. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 16-33.

For the above reasons, it is believed that the rejections of claims 17-20, 23 and 28-33 under 35 U.S.C. § 103(a) based on Ogawa, *et al.* and Kai, *et al.*, is improper, and reconsideration and removal of the rejections are respectfully requested.

In the present invention as claimed in claims 34-36, a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate, a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-intermetal dielectric and an alignment key formed only in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor.

With regard to the rejection of claims 14-26 and 34-36 as being unpatentable over Yoshitomi and Ning, *et al.*, is stated in the Office Action at pages 6 and 7, section 10, that Yoshitomi fails to teach forming an alignment key in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor and the key comprising the metal layer for the lower electrode, the dielectric layer, and the metal

layer for the upper electrode on the inner walls of the alignment key. Therefore, Yoshitomi fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes an alignment key formed only in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor, as claimed in claims 34-36.

Ning, *et al.* discloses that an insulating layer 20 is patterned and etched to form areas or trenches that define a pattern 22 for a plurality of conductive lines in the conductive region 12, a pattern 24 for at least one alignment mark 24 in the alignment mark region 14, and a pattern 30 for at least one MIM capacitor in the MIM capacitor region 16 (see Ning, *et al.*, column 4, liens 60-65). In Ning, *et al.*, the process may be single or dual damascene. In a dual damascene process the alignment mark 24 includes the depth 26 of metal wiring plus the depth of vias. Therefore, the alignment mark 24 is formed in a trench-level insulating layer in both a single and dual damascene process, not only in a via-level intermetal dielectric as claimed.

Ning, *et al.*, like Yoshitomi, fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. In addition, like Yoshitomi, Ning, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes an alignment key formed only in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor, as claimed in claims 34-36. Instead, the alignment mark 24 of Ning, *et al.* is formed in a trench in the insulating layer 20.

Yoshitomi and Ning, *et al.* fail to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Yoshitomi and Ning, *et al.* fail to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33 and a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes an alignment key formed only in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal

capacitor, as claimed in claims 34-36. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 16-33 and 34-36. Therefore, it is believed that claims 16-33 and 34-36 are allowable over the cited references, and reconsideration of the rejections of claims 14-26 and 34-36 under 35 U.S.C. § 103(a) based Yoshitomi and Ning, *et al.*, is respectfully requested.

New claims 37-39 are added. Claims 37-39 recite that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a lower electrode which is directly connected to a first lower metal interconnection. None of the cited references teaches or suggests a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a lower electrode which is directly connected to a first lower metal interconnection. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 37-39. Therefore, it is believed that claims 37-39 are allowable.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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